What is claimed is:

1. An apparatus for controlling an output current (I_{OUT}) that is delivered to a load circuit from an inductor, the apparatus comprising:

a transistor switching circuit that is arranged to selectively couple a switch node to a power supply when activated, such that the inductor is charged by an input voltage (V_{IN}) when the transistor switching circuit is activated, wherein the inductor is arranged to deliver the output current (I_{OUT}) to the load circuit when the transistor switching circuit is deactivated;

a ramp generator circuit that is arranged to provide a ramp signal (V_{RAMP}), wherein the ramp signal (V_{RAMP}) is reset to a predetermined level in response to a reset signal (ENR);

a comparator circuit that is arranged to compare the ramp signal (V_{RAMP}) to a reference signal (V_{REF})to provide a comparison signal (V_{COMP}), wherein the comparison signal (V_{COMP}) is asserted when the ramp signal (V_{RAMP}) exceeds the reference signal (V_{REF});

a feed-forward circuit that is arranged to activate a pulse signal (V_{FF}) when the voltage (V_{SW}) associated with the switch node decreases by a predetermined amount; and

a latch circuit that is arranged to: assert the reset signal (ENR) when the pulse signal (V_{FF}) is asserted, activate the transistor switching circuit when the reset signal (ENR) and the comparison signal (V_{COMP}) are de-asserted, and deactivate the transistor switching circuit when the comparison signal (V_{COMP}) is asserted.

2. The apparatus of Claim 1, wherein the power supply corresponds to at least one of a high power supply, a low power supply, and a circuit ground.

3. The apparatus of Claim 1, further comprising a start-up circuit that is arranged to initialize the latch circuit during a start-up sequence.

4. The apparatus of Claim 1, further comprising a start-up circuit that is arranged to activate the inductor during a start-up sequence such that the inductor is initialized to an appropriate condition.

5. The apparatus of Claim 1, wherein the ramp generator circuit is further arranged such that a slope associated with the ramp signal (V_{RAMP}) is determined by an adjustable parameter (X) and the input voltage (V_{IN}) such that the slope is proportional to $X*V_{IN}^2$.

6. The apparatus of Claim 1, wherein the transistor switching circuit is further arranged such that the output current (I_{OUT}) that is delivered to the load circuit is inversely proportional to $L*V_{OUT}$, where L corresponds to a value associated with the inductor and V_{OUT} corresponds to the output voltage that is associated with the load circuit.

7. The apparatus of Claim 1, further comprising: a resistor that is arranged to cooperate with the ramp generator circuit such that a value (R_{SET}) associated with the resistor adjusts the slope of the ramp signal (V_{RAMP}), wherein the ramp generator circuit and the comparator circuit are arranged to cooperate with the feed-forward circuit such that an on-time (T_{ON}) associated with the transistor switching circuit is adjusted by changing the slope of the ramp signal.

8. The apparatus of Claim 7, wherein the transistor switching circuit is arranged to cooperate with the inductor such that the output current (I_{OUT}) is inversely proportional to $L*R_{SET}$.

9. The apparatus of Claim 1, wherein the ramp generator circuit comprises a capacitor (C_R) that is charged by a current source (CS) when the reset signal is de-asserted.

10. The apparatus of Claim 9, further comprising a resistor that is arranged to cooperate with the ramp generator circuit such that a current level (I_{MATH}) associated with the current source (CS) is responsive to a value (R_{SET}) associated with the resistor.

11. The apparatus of Claim 9, further comprising a resistor that is arranged to cooperate with the ramp generator circuit such that a current level (I_{MATH}) associated with the current source (CS) is proportional to $R_{SET}*V_{IN}^2$, wherein the resistor has a value corresponding to R_{SET}.

12. An apparatus for controlling an output current (I_{OUT}) that is delivered to a load circuit from an inductor, the apparatus comprising:

a switching means that is arranged to selectively couple a switch node to a power supply node when activated, such that the inductor is charged by an input voltage (V_{IN}) when the switching means is activated, wherein the inductor is arranged to deliver the output current (I_{OUT}) to the load circuit when the switching means is deactivated;

a ramp means that is arranged to provide a ramp signal (V_{RAMP}), wherein the ramp means is arranged to initialize the ramp signal (V_{RAMP}) to a predetermined level in response to a reset signal (ENR);

a comparison means that is arranged to compare the ramp signal (V_{RAMP}) to a reference signal (V_{REF})to provide a comparison signal (V_{COMP}), wherein the comparison signal (V_{COMP}) is asserted when the ramp signal (V_{RAMP}) reaches the reference signal (V_{REF});

a sense means that is arranged to activate a pulse signal (V_{FF}) when the voltage (V_{SW}) associated with the switch node is sensed as decreasing by a predetermined amount; and

a latch means that is arranged to: assert the reset signal (ENR) when the pulse signal (V_{FF}) is asserted, activate the switching means when the reset signal (ENR) and the comparison signal (V_{COMP}) are de-asserted, and deactivate the switching means when the comparison signal (V_{COMP}) is asserted.

13. The apparatus of Claim 12, wherein the ramp means is further arranged such that a slope associated with the ramp means is determined by an adjustable parameter (X) and the input voltage (V_{IN}) such that the slope is proportional to $X*V_{IN}^2$.

14. The apparatus of Claim 12, further comprising: a resistor means that is arranged to cooperate with the ramp means such that a value (R_{SET}) associated with the resistor means adjusts the slope of the ramp signal (V_{RAMP}), wherein the ramp means and the comparison means are arranged to cooperate with the sense means such that an on-time (T_{ON}) associated with a charging cycle of the inductor is adjusted by changing the slope of the ramp signal.

15. The apparatus of claim 12, wherein the ramp means is arranged such that the ramp signal (V_{RAMP}) is a decreasing signal and the predetermined level corresponds to a high power supply level.

16. The apparatus of claim 12, wherein the ramp means is arranged such that the ramp signal (V_{RAMP}) is an increasing signal and the predetermined level corresponds to a low power supply level.

17. A method for providing a current (I_{OUT}) to a load circuit from an inductor, the method comprising:

evaluating a switch signal (V_{SW}), wherein the switch signal is associated with the inductor;

monitoring a ramp signal (V_{RAMP}), wherein the ramp signal (V_{RAMP}) has a magnitude that varies over time according to a slope;

resetting the ramp signal (V_{RAMP}) to a reset level when the switch signal (V_{SW}) drops below a predetermined level;

controlling an on-time interval in response to the ramp signal (V_{RAMP}) and a reference signal level (V_{REF}), wherein the on-time is related to the slope of the ramp signal (V_{RAMP});

charging the inductor with an input voltage (V_{IN}) over the on-time interval (T_{ON}); and

coupling current from the inductor to the load circuit when the ramp signal level has reached the reference signal level.

18. The method of claim 17, further comprising: identifying requirements associated with the load circuit, and changing the slope of the ramp in response to the identified load requirements, wherein the requirements corresponds to at least one of the operating voltage across the load circuit and the operating current requirements for the load circuit.

19. The method of claim 17, adjusting the slope of the ramp signal in response to a parameter (X) and the input voltage (V_{IN}) such that the slope of the ramp signal (V_{RAMP}) is proportional to $X*V_{IN}^2$.

20. The method of claim 17, wherein the ramp signal is a decreasing signal that decreases at a rate that is determined by the slope of the ramp signal such that the on-time interval (T_{ON}) spans the time period from the of the reset of the ramp signal until the time where the ramp signal reaches the reference signal level (V_{REF}).